WHAT IS CLAIMED IS:

1. A chip package structure, comprising:

a glass substrate having a substrate surface;

a circuit layer on said substrate surface, wherein said circuit layer includes a plurality of first bonding pads and a plurality of second bonding pads on a surface of said circuit layer;

at least a die having an active surface and a back side, wherein said die includes a plurality of die pads on said active surface;

a plurality of bumps, wherein each of said bumps connects one of said die pads with one of said first bonding pads; and

a plurality of contacts disposed on said second bonding pads.

2. The chip package structure of claim 1, further comprising an insulated material applied between said circuit layer and said die.

3. The chip package structure of claim 1, wherein said circuit layer is a patterned conductive layer, which forms said first bonding pads and said second bonding pads.

4. The chip package structure of claim 1, wherein said circuit layer includes a plurality of patterned conductive layers, at least a dielectric layer and at least a conductive via, said conductive layers are set on said substrate surface, said dielectric layer is set between said conductive layers, said conductive via penetrating through said dielectric layer electrically connects said conductive layers, and one of said conductive layers farthest from said glass substrate forms said first bonding pads and said second bonding pads.

5. The chip package structure of claim 1, wherein said contacts are balls or

pins.

6. The chip package structure of claim 1, further comprising at least an active device inside said circuit layer and disposed on said substrate surface.

7. The chip package structure of claim 1, further comprising at least a passive device inside said circuit layer.

8. The chip package structure of claim 1, further comprising at least a passive device on the surface of said circuit layer.

9. The chip package structure of claim 1, further comprising a heat-conducting layer on said back side of said die.

10. The chip package structure of claim 9, wherein said heat-conducting layer is a heat spreader or a conducting paste layer.

11. The chip package structure of claim 10, further comprising a carrier, wherein said carrier includes a carrier surface, at least a first carrier pad and a plurality of second carrier pads, and said die connects to said first carrier pad via said heat-conducting layer, and said contacts respectively connect to said second carrier pads.

12. The chip package structure of claim 10, wherein said heat-conducting layer includes electrically conductive material, and said first carrier pad is a ground pad so that said die is electrically coupled to said first carrier pad via said heat-conducting layer.

13. A chip package structure, comprising

a glass substrate having a substrate surface;

a circuit layer on said substrate surface, wherein said circuit layer includes a plurality of first bonding pads and a plurality of second bonding pads on the surface of said circuit layer;

at least a die having an active surface and a back side, wherein said back side of said die is set on said circuit layer and said die includes a plurality of die pads on said active surface;

a plurality of conducting wires, wherein each of said conducting wire connects one of said die pads with one of said first bonding pads; and

a plurality of contacts disposed on said second bonding pads.

14. The chip package structure of claim 13, further comprising an insulated material covering said die and said conducting wires.

15. The chip package structure of claim 13, wherein said circuit layer is a patterned conductive layer, which forms said first bonding pads and said second bonding pads.

16. The chip package structure of claim 13, wherein said circuit layer includes a plurality of patterned conductive layers, at least a dielectric layer and at least a conductive via, said conductive layers are set on said substrate surface, said dielectric layer is set between said conductive layers, said conductive via penetrating through said dielectric layer electrically connects said conductive layers, and one of said conductive layers farthest from said glass substrate forms said first bonding pads and said second bonding pads.

17. The chip package structure of claim 13, wherein said contacts are balls or pins.

18. The chip package structure of claim 13, further comprising at least an active device inside said circuit layer and above said substrate surface.

19. The chip package structure of claim 13, further comprising at least a passive device inside said circuit layer.

20. The chip package structure of claim 13, further comprising at least a passive device on the surface of said circuit layer.

21. A chip package structure, comprising:

a glass substrate having a substrate surface;

a circuit layer on said substrate surface, wherein said circuit layer has an interconnection structure;

at least a die on said circuit layer, wherein said die is coupled to said interconnection structure; and

a plurality of contacts on said circuit layer, wherein said contacts are coupled to said interconnection structure.

22. The chip package structure of claim 21, wherein said circuit layer is a patterned conductive layer, which forms said interconnection structure.

23. The chip package structure of claim 21, wherein said circuit layer includes a plurality of patterned conductive layers, at least a dielectric layer and at least a conductive via, said conductive layers are set on said substrate surface, said dielectric layer is set between said conductive layers, said conductive via penetrating through said dielectric layer electrically connects said conductive layers, and said conductive layers and said conductive via form said interconnection structure.

24. The chip package structure of claim 21, said die is coupled to said interconnection structure by using flip chip technology.

25. The chip package structure of claim 21, said die is coupled to said interconnection structure by using wire bonding technology.

26. The chip package structure of claim 21, wherein said contacts are balls or pins.

27. The chip package structure of claim 21, further comprising at least an active device inside said circuit layer and disposed on said substrate surface.

28. The chip package structure of claim 21, further comprising at least a passive device inside said circuit layer.

29. The chip package structure of claim 21, further comprising at least a passive device on the surface of said circuit layer.